CLAIMS

1. A nonvolatile semiconductor storing device comprising:

a memory array including a plurality of memory blocks that consists of nonvolatile memory cells arranged in the form of an array in which program and erase operations can be electrically performed and can be erased in block and a redundant block having the same number of memory cells and the same constitution as that of one of the memory blocks; and

a block replacing means for replacing a defective block with the redundant block in a case where one of the memory blocks in the memory array is the defective block, wherein

the block replacing means includes an address translation circuit for converting an inputted external block address into an internal block address by inverting an address bit corresponding to dissidence of each address bit between a defective block address of the defective block and the redundant block address among address bits of the inputted external block address, and

each of the memory blocks is selected based on the internal block address after the translation of the external block address inputted from outside by the address translation circuit.

2. The nonvolatile semiconductor storing device according to Claim 1, wherein

a particular block address of one particular memory block in the memory array is overlapped with a redundant block address of the redundant block, and

the block replacing means includes a particular block address

detection circuit for detecting whether the block address inputted from outside is the particular block address or not and outputting a signal for forcibly selecting the particular memory block when the block address coincides with the particular block address.

3. The nonvolatile semiconductor storing device according to Claim 2, wherein the particular memory block is a boot block constituted by a plurality of small memory blocks allowing data to be erased in block.

4. The nonvolatile semiconductor storing device according to Claim 3, wherein a body part of the memory array includes the redundant block and the memory blocks other than the boot block, and

the boot block is disposed away from the memory array body part.

5. The nonvolatile semiconductor storing device according to Claim 2, wherein the particular block address is a most significant or least significant address of the block addresses.

6. The nonvolatile semiconductor storing device according to Claim 1, wherein

the block replacing means includes a defective block address memory circuit for storing information regarding the defective block address or dissidence of each address bit between the defective block address and the redundant block address, and

the address translation circuit includes one of an exclusive NOR

circuit and an exclusive OR circuit for each address bit of the block address.

7. The nonvolatile semiconductor storing device according to Claim 6, wherein the defective block address memory circuit is writable from outside.

8. The nonvolatile semiconductor storing device according to Claim 1, wherein the memory array is configured to be divided into a plurality of partitions each including the plurality of memory blocks, and

during a write operation to a memory block in the partition, a reading operation to a memory block in another one of the partitions is allowed to be performed.

9. The nonvolatile semiconductor storing device according to Claim 1, wherein the memory cell is a floating gate type of flash memory cell.

10. A block redundancy saving method for a nonvolatile semiconductor storing device comprising a memory array including a plurality of memory blocks that consists of nonvolatile memory cells arranged in the form of an array in which program and erase operations can be electrically performed and can be erased in block, and a redundant block having the same number of memory cells and the same constitution as that of one of the memory blocks, the method comprising:

an address translating step for converting an external block address inputted from outside into an internal block address by inverting an address

bit corresponding to dissidence between a defective block address of the defective block and the redundant block address among address bits of the external block address inputted from outside; and

a memory block selecting step for selecting the memory block using the internal block address.

11. The block redundancy saving method according to Claim 10, wherein

a particular block address of one particular memory block in the memory array is overlapped with a redundant block address of the redundant block, and

whether the external block address inputted from outside is the particular block address or not is detected, and the particular memory block is forcibly selected when the external block address coincides with the particular block address.